IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of: Docket No. P27157

Haujie CHEN, *et al.* Confirmation No. 4303

Group Art Unit: 2813

Appln. No. : 10/689,506

Examiner: N. O. Berezny

Filed : October 20, 2003

For : HIGH PERFORMANCE STRESS-ENHANCED MOSFETs USING Si:C AND SiGe EPITAXIAL SOURCE/DRAIN AND METHOD OF MANUFACTURE

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria VA 22314

AMENDMENT UNDER 37 C.F.R. §1.112

Sir:

In response to the non-final Office Action dated April 11, 2006, Applicants request reconsideration of the rejected claims in view of the following amendments and remarks.

Amendments to the claims begin on page 2; and

Remarks begin on page 7.

If extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefore (including fees for net addition of claims) are hereby authorized to be charged to Deposit Account No. 09-0458.

AMENDMENT TO THE CLAIMS

Please **AMEND** claims 1, 7 and 10; and

Please **ADD** new claims 22-25 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A method of manufacturing a semiconductor structure, comprising the steps of:

forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate;

forming a pFET stack in the pFET channel and an nFET stack in the nFET channel;

after the pFET stack is formed, providing a first layer of material at source/drain regions associated with the pFET stack, the first layer of material having a lattice constant different than a base lattice constant of the substrate to create a compressive state within the pFET channel; and

after the nFET stack is formed, providing a second layer of material at the source/drain regions associated with the nFET stack, the second layer of material having a lattice constant different than the base lattice constant of the substrate to create a tensile state at the nFET channel.

2. (Original) The method of claim 1, wherein the first layer of material is SiGe having a content of Ge approximately greater than 0% in ratio to Si.

3. (Original) The method of claim 1, wherein the second layer of material is Si:C.

4. (Original) The method of claim 3, wherein the Si:C has a content of C of about 4% or less.

5. (Previously Presented) The method of claim 1, wherein the first layer of material is unrelaxed SiGe and the second layer of material is unrelaxed Si:C and each of the first and second layers of material is formed at a thickness of between about 10 to 100 nm.

6. (Original) The method of claim 1, wherein:

the first layer of material is formed by placing a mask over the nFET channel and etching the regions of the pFET and selectively growing the first layer of material within the regions of the pFET channel; and

the second layer of material is formed by placing a mask over the pFET channel and etching regions of the nFET and selectively growing the second layer of material within the regions of the nFET channel.

7. (Currently Amended) ~~The method of claim 6, further comprising the steps of:~~ A method of manufacturing a semiconductor structure, comprising the steps of:

forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate;

forming a pFET stack in the pFET channel and an nFET stack in the nFET channel;

providing a first layer of material at source/drain regions associated with the pFET stack, the first layer of material having a lattice constant different than a base lattice constant of the substrate to create a compressive state within the pFET channel; and

providing a second layer of material at the source/drain regions associated with the nFET stack, the second layer of material having a lattice constant different than the base lattice constant of the substrate to create a tensile state at the nFET channel;

the first layer of material being formed by placing a mask over the nFET channel and etching the regions of the pFET and selectively growing the first layer of material within the regions of the pFET channel, and the second layer of material being formed

by placing a mask over the pFET channel and etching regions of the nFET and selectively growing the second layer of material within the regions of the nFET channel;

providing a protection layer under the mask and over the nFET stack prior to the etching of the regions of the pFET stack and selectively growing the first layer of material; and

providing a protection layer under the mask and over the nFET stack prior to the etching of the regions of the pFET stack and selectively growing the second layer of material.

8. (Previously Presented) The method of claim 1, wherein the first layer of material and the second layer of material are each grown to a thickness about 10 to 100 nm.

9. (Original) The method of claim 1, wherein the first layer of material and the second layer of material are embedded in the layer.

10. (Currently Amended) A method of manufacturing a semiconductor structure, comprising the steps of:

forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate;

forming a pFET structure and an nFET structure on the substrate associated with the pFET channel and the nFET channel, respectively; etching regions of the pFET structure and the nFET structure;

after the pFET stack is formed, forming a first material with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress in the pFET channel;

after the nFET stack is formed, forming a second material with a lattice constant different than the base lattice constant of the substrate in the regions of the nFET structure to provide a tensile stress in the nFET channel; and

doping source and drain regions of the nFET and pFET structures.

11. (Original) The method of claim 10, wherein the first material is SiGe and the second material is Si:C.

12. (Previously Presented) The method of claim 10, wherein:
the first material creates a compressive stress within the pFET channel; and
the second material creates a tensile stress within the nFET channel.

13. (Previously Presented) The method of claim 10, wherein:
the first material is formed by placing a protective layer over the nFET structure and the pFET structure and growing the first material within source and drain regions of the pFET channel; and
the second material is formed by placing a protective layer over the pFET structure and source and drain regions of the pFET structure and the nFET structure and growing the second material within source and drain regions of the nFET channel.

14. (Previously Presented) The method of claim 10, wherein the first material and the second material are embedded in the substrate.

15. (Previously Presented) The method of claim 10, wherein the first material and the second material are raised above a surface of the substrate.

16. (Previously Presented) The method of claim 10, wherein the first material and the second material each have a thickness of between about 10 to 100 nm.

17. (Original) The method of claim 10, wherein the first material is unrelaxed SiGe.

18. (Original) The method of claim 10, further comprising the step of in situ doping the first material with p-type doping and the second material with n-type doping to form the source and drain regions of the pFET and nFET, respectively.

Claims 19-21 (Canceled).

22. (New) A method of manufacturing a semiconductor structure, comprising the steps of:

forming a pFET stack and an nFET stack on a substrate;

forming channels in the substrate about the pFET stack;

growing a layer of material in the channels associated with the pFET stack, wherein after the growing, the layer of material has a lattice structure that tends to match a lattice structure of an underlying portion of the substrate to create a compressive state within the channels of the pFET stack;

forming channels in the substrate about the nFET stack; and

growing a layer of material in the channels associated with the nFET stack, wherein after the growing, the layer of material has a lattice structure that tends to match a lattice structure of an underlying portion of the substrate to create a tensile state within the channels of the nFET stack.

23. (New) The method of claim 22, wherein:

before the layer of material in the channels associated with the pFET is grown, the layer of material has a lattice constant different than a base lattice constant of the substrate; and

before the layer of material in the channels associated with the nFET is grown, the layer of material has a lattice constant different than a base lattice constant of the substrate.

24. (New) The method of claim 22, wherein the channels about the pFET stack and the channels about nFET stack are formed by etching.

25. (New) The method of claim 22, wherein the channels about the pFET stack and the channels about the nFET comprise source/drain regions.

REMARKS

Claims 1-18 and 22-25 are currently pending in the application. Claims 1, 7 and 10 have been amended and claims 22-25 have been added. Support for new claims 22-24 can be found at paragraphs [0024] and [0033] of the instant published patent application No. 2005/0082616. No new matter has been added. Reconsideration of the rejected claims in view of the following remarks is respectfully requested.

Allowable Claims

Applicants appreciate the indication that claim 7 contains allowable subject matter. Accordingly, as Applicants are presenting this claim in independent form, Applicants request that at least claim 7 be indicated to be allowed. Furthermore, Applicants submit that all of the claims are in condition for allowance for the following reasons.

35 U.S.C. §102 Rejection

Claims 1-4, 8-12, 14, 16 and 17 were rejected under 35 U.S.C. §102(e) over US Patent No. 6,774,409 to BABA et al. The rejection is respectfully traversed.

In order to establish a *prima facie* case of anticipation under 35 U.S.C. § 102, a single prior art reference must disclose each and every element as set forth in the subject claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). Applicants respectfully submit that a *prima facie* case of anticipation cannot be established because BABA fails to teach each and every element of the claims.

More particularly, independent claim 1 recites, *inter alia,*

after the pFET stack is formed, providing a first layer of material at source/drain regions associated with the pFET stack, the first layer of material having a lattice constant different than a base lattice constant of the substrate to create a compressive state within the pFET channel; and
after the nFET stack is formed, providing a second layer of material at the source/drain regions associated with the nFET stack, the second layer of material having a lattice constant different than the base lattice constant of the substrate to create a tensile state at the nFET channel.

Additionally, independent claim 10 recites, *inter alia,*

after the pFET stack is formed, forming a first material with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress in the pFET channel;
after the nFET stack is formed, forming a second material with a lattice constant different than the base lattice constant of the substrate in the regions of the nFET structure to provide a tensile stress in the nFET channel.

Applicants submit that BABA does not disclose or even suggest at least these features. Applicants acknowledge that BABA discloses the forming of an SiGe layer 4 and a carbon Si film 5 on a substrate which will support nFET and pFET devices (see Figs. 1(a) – 1(d)). Applicants also acknowledge that BABA discloses that the layers 4 and 5 can have different lattice constants than the substrate and that the layer 4 can form compression in the pFET and that the layer 5 can form strain distortion in the nFET (see col. 6, lines 39-67). However, Applicants submit that BABA does not disclose, or even suggest, that the layers 4 and 5 are formed after the pFET and nFET stacks are formed. To the contrary, Figs. 1a-1d clearly show that the layers 4 and 5 are formed or grown before to the formation of the pFET and nFET stacks.

Thus, Applicants respectfully submit that independent claims 1 and 10, as well as claims 2-4, 8, 9, 11, 12, 14, 16 and 17, which depend from claims 1 and 10 are allowable.

Accordingly, Applicants respectfully request that the above-noted rejection under 35 U.S.C. § 102(e) should be withdrawn.

35 U.S.C. §103 Rejection

Claims 1-6, 8, 10-13 and 15-18 were rejected under 35 U.S.C. §103(a) over US Patent Application Publication No. 2005/0035470 to KO et al. in view of US Patent Application Publication No. 2003/0080361 to MURTHY et al. The rejection is respectfully traversed.

Applicants submit that this basis of rejection is improper at least because KO is not prior art. As the Examiner knows, Applicants have established, by Rule 1.131 Declaration, an effective filing date in the previous response of at least June 17, 2003. On the other hand, KO was filed in the US on August 12, 2003, i.e., after June 17, 2003. Thus, regardless of what KO and MURTHY discloses or suggests, KO does not qualify as prior art under 35 U.S.C. § 102 and the instant rejection is therefore improper.

Accordingly, Applicants respectfully request that the above-noted §103(a) rejection of claims 1-6, 8, 10-13 and 15-18 be withdrawn.

Comments on Reasons for Allowance

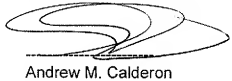
In response to the Statement of Reasons for Allowance set forth in the Office Action, Applicants wish to clarify the record with respect to the basis for the patentability

of the indicated claim in the present application. In this regard, while Applicant does not disagree with the Examiner's indication that certain identified features are not disclosed by the references, Applicants submit that the allowed claim in the present application recites a combination of features, and that the basis for patentability of this claim is based on the totality of the recited features.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0458.

Respectfully submitted,
Haujie CHEN, *et al.*



Andrew M. Calderon
Reg. No. 38,093

July 11, 2006
GREENBLUM & BERNSTEIN, P.L.C.
1950 Roland Clarke Place
Reston, VA 20191
(703) 716-1191